Amendment to the claims

Please cancel claim 17, and amend claims 1-5, 7-14, 16 and 20 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) A memory device comprising:

a. a memory ~~(EM)~~ having at least two predetermined register memory sections addressable by respective address ranges ~~(AS1 to ASz)~~;

b. at least one access port ~~(Pi to PZ)~~ for providing access to said memory ~~(EM)~~; and

c. access control means ~~(A)~~ for addressing said memory ~~(EM)~~ so as to operate said register memory sections as shift registers and to map shift register accesses of said at least one access port ~~(P1 to PZ)~~ to predetermined addresses in [[the]] a global address space of said memory, said control means being external to said memory and being configured to generate memory addresses for writing to and reading from said memory ~~(EM)~~.

2. (currently amended) A device according to claim 1, wherein said access control means ~~(A)~~ comprises at least one address counter.

3. (currently amended) A device according to claim 1, wherein said address ranges ~~(AS1 to ASz)~~ comprise overlapping regions of a predetermined size.

4. (currently amended) A device according to claim 1, wherein said at least one access port ~~(P1 to PZ)~~ provides access to a plurality of data sources for writing data to respective ones of said register memory sections, and to a plurality of data processing devices for reading data from said register memory sections.

5. (currently amended) A device according to claim 4, wherein said access control means ~~(A)~~ is arranged to provide alternate access for said data sources and said data processing devices.

6. (previously presented) A device according to claim 4, wherein data source accesses are controlled to cycle through said global address space, and processing device accesses are controlled to cycle through the address range of a respective register memory section.

7. (currently amended) A device according to claim 1, further comprising a buffer memory ~~(B)~~ connectable to said at least one access port ~~(P1 to PZ)~~ and to said memory ~~(EM)~~, wherein a line width of said buffer memory ~~(B)~~ and said memory ~~(EM)~~ is selected to be greater or equal the data width of said at least one access port multiplied by the sum of read accesses and write accesses per cycle.

8. (currently amended) A device according to claim 7, wherein said memory ~~(EM)~~ is a single-port memory.

9. (currently amended) A device according to claim 7, wherein said at least one access port ~~(P1 to PZ)~~ comprises a plurality of write ports and a plurality of read ports, wherein the number of write ports differs from the number of read ports.

10. (currently amended) A device according to claim 7, wherein said buffer memory ~~(B)~~ is arranged to buffer read and write accesses of said at least one access port ~~(P1 to PZ)~~.

11. (currently amended) A device according to claim 7, wherein said address control means ~~(A)~~ comprises address translation means ~~(AC)~~ for aligning addresses relating to said read accesses in such a way that they fit to said line width.

12. (currently amended) A device according to claim 11, wherein said address translation means ~~(AC)~~ comprises a look-up table ~~(LUT)~~.

13. (currently amended) A device according to claim 7, wherein said access control means ~~(A)~~ is adapted to transfer write accesses to said buffer memory ~~(B)~~ until it is full, and to write one memory line when said buffer memory ~~(B)~~ is full.

14. (currently amended) A device according to claim 7, wherein said address control means ~~(A)~~ is adapted to align read accesses in such a way that a block of said line width is read all the time.

15. (previously presented) A device according to claim 1, wherein said at least two predetermined register memory sections are operated as FIFO memory sections.

16. (previously presented) A demultiplexing device for demultiplexing a plurality of input data streams and supplying demultiplexed data streams to a plurality of data processing units, said input data streams being supplied to a memory device, said memory device comprising:

a memory having at least two predetermined register memory sections addressable by respective address ranges;

at least one access port for providing access to said memory; and

access control means for addressing said memory so as to operate said register memory sections as shift registers and to map shift register accesses of said at least one access port to predetermined addresses in a global address space of said memory,

wherein said demultiplexing device comprises a PRML-based interleaver functionality ~~as claimed in claim 1~~.

17. (canceled).

18. (previously presented) A multiplexing device for multiplexing data streams supplied from a plurality of data processing units, and for generating multiplexed output data streams, said data streams being supplied to a memory device as claimed in claim 1.

19. (original) A device according to claim 18, wherein said multiplexing device comprises a PRML-based de-interleaver functionality.

20. (currently amended) A method comprising the steps of:

providing a memory ~~(EM)~~ having at least two predetermined register memory sections addressable by respective address ranges ~~(AS1 to ASz)~~;

providing at least one access port ~~(P1 to PZ)~~ for providing access to said memory ~~(EM)~~; and

providing access control means ~~(A)~~ for addressing said memory ~~(EM)~~ so as to operate said register memory sections as shift registers and to map shift register accesses of said at least one access port ~~(P1 to PZ)~~ to predetermined addresses in [[the]] a global address space of said memory, said control means being external to said memory and being configured to generate memory addresses for writing to and reading from said memory ~~(EM)~~.